Hello from Werner Feith and I hope, despite we did not talk for quite some time, you are well. Just before the end of January 2025 and after Chinese New Year I wanted to show up again and wish you all the best for the upcoming eastern as western new year!

I made up my mind to publish a somehow regular newsletter on, in the meantime my hobby, machine-vision-interfaces. I have your data from my pool of data collected over the years with my Sensor-to-Image ownership and my time at EMVA, the European Machine Vision Association, but if you do not like to receive these news just answer to this mail with the single word "UNSUBSCRIBE" in the text of your mail and you will be removed from this list - sorry to bother!

Being now again in the IVSM meetings, the GenICam working group and visiting shows with machine vision technology I feel I can add some of my single-senior-experience-view to the mainstream machine-vision-marketing news. Here is my first input on MV-interface technology for the upcoming year of 2025: High speed image transmission with the focus on reliable data delivery (to distinguish from secure data, as reliable data can still be hacked)

The solution for physical data reliability on the wire are right now RoCEv2 and MIPI A-PHY. These should be the preferred technologies for the machine vision interface, which can run on BER, bit error rate, of less than 10e-20, due to their embedded mechanisms of line-tuning and data retransmission, which is simply missing in U3V, CXP and CLHS. GEV V1 and V2 has some data-checking and retransmission implemented on upper protocol layer, but this specification did not really work as shown over the different implementations especially on speed >5Gbps – GEV V3, to be released in 2025, is built on RoCEv2, and A-PHY/ IEEE-2977 might be adapted by machine vision soon!

Why now mentioning BER - running an interface at 10Gbit/sec=10e10 bps and copper cable/connector lab-environment BER of 10-e12 to 10e-14 generates random errors each 100 to 10000sec, which can cause a corrupt image about in between 2 minutes to 3 hours. If you run in high EMC, Electro- Magnetic Compatibility, environments like robot-arms, BER can 1000 times lower and so the image corruption rate 1000 times higher, which is not acceptable for any machine vision application.

Maybe you argue in this situation that fiber connectivity can solve the copper BER problem – and the answer is not really. Fiber connections do not interfere a lot with EMC noise, but the basic system BER of fiber connections is like copper connectivity and not the solution needed for reliable multi-gigabit image data delivery in noisy 24/7/365 environments.

The big step is embedded line-tuning and data-checking/retransmission available on RoCEv2 and MIPI A-PHY with e.g. these vendors and locations:
EmbededWorld, 11-13.3.2025 in Nuremberg: imavix engineering, RoCEv2 on Efinix FPGA, Hall 2 / Booth Number 2-412
EmbededWorld, 11-13.3.2025 in Nuremberg: Sensor to Image, RoCEv2 on Altera FPGA, Hall 2 / Booth Number 2-552
EmbededWorld, 11-13.3.2025 in Nuremberg: Valens Semiconductor Ltd., A-PHY Silicon, Hall 2 / Booth Number 2-454
Shanghai Vision Show, 26-28.3.2025 in Shanghai/China: imavix engineering, RoCEv2 on Efinix FPGA, G3 standards booth

And if you like to know more details, just let me know at my regular mail address: werner@mevg.org - hope to see you in Nuremberg or Shanghai.

Best Regards, Werner Feith

PS.: here are a few links maybe worth reading on BER out- and inside machine vision industry

Nice explanation of basic BER: https://www.fiberoptics4sale.com/blogs/archive-posts/95047174-what-is-ber-bit-error-ratio-and-bert-bit-error-ratio-tester

Overview fiber BER, sources of failures and BERT=BER Testing: https://www.occfiber.com/x_upload/news/files/1469115240_05052016_White_Paper_-_(BERT)_Bit_Error_Rate_Testing.pdf

System BER on fiber: https://www.researchgate.net/publication/51193543_Bandwidth_measurement_of_multimode_fibers_using_system_level_bit_error_rate_testing

FEC for CoF, CXP over fiber:
https://www.xilinx.com/products/intellectual-property/ef-di-clause74-fec.html
https://www.intel.com/content/www/us/en/docs/programmable/683171/current/forward-error-correction-clause-74.html